AMENDMENTS

In the Claims:

1. (Currently Amended) A testing method for testing contacting between a semiconductor ~~device~~ chip and a carrier, comprising:

loading the carrier with the semiconductor ~~device~~ chip,

wherein the contacting between the carrier and the semiconductor ~~device~~ chip is tested immediately after the loading of the carrier with the semiconductor ~~device~~ chip, and

wherein the semiconductor ~~device~~ chip comprises one or more contacting test contacts exclusively for testing the contacting between the semiconductor ~~device~~ chip and the carrier.

2. (Original) The testing method according to claim 1, further comprising connecting the carrier to a testing apparatus.

3. (Currently Amended) The testing method according to claim 2, wherein the carrier is connected to the testing apparatus, and the carrier is subsequently loaded with the semiconductor ~~device~~ chip.

4. (Currently Amended) The testing method according to claim 1, wherein the carrier is loaded at a carrier loading station, and the contacting between the carrier and the semiconductor ~~device~~ chip is tested before the carrier is transported to a further station.

5. (Currently Amended) The testing method according to claim 2, wherein the contacting between the carrier and the semiconductor ~~device~~ chip is tested by the testing apparatus.

6. (Currently Amended) The testing method according to claim 5, wherein the testing apparatus is configured such that it tests the contacting between the carrier and the semiconductor ~~device~~ chip, but not functioning of the semiconductor ~~device~~ chip.

7. (Currently Amended) The testing method according to claim 1, wherein the contacting between the carrier and the semiconductor ~~device~~ chip is tested less than 2 seconds after loading of the carrier with the semiconductor ~~device~~ chip.

8. (Currently Amended) The testing method according to claim 1, further comprising determining during the testing of the contacting between the carrier and the semiconductor ~~device~~ chip whether an electric contact has been established between a corresponding pad of the semiconductor ~~device~~ chip and an assigned pad of the carrier after loading of the carrier with the semiconductor ~~device~~ chip.

9. (Currently Amended) The testing method according to claim 1, further comprising determining during the testing of the contacting between the carrier and the semiconductor ~~device~~ chip whether a respective electric contact has been established between a plurality of pads of the semiconductor ~~device~~ chip and respectively assigned pads of the carrier after loading of the carrier with the semiconductor ~~device~~ chip.

10. (Currently Amended) The testing method according to claim 8, wherein power of current flowing through the corresponding semiconductor ~~device~~ chip pad is determined to find whether an electric contact has been established between a corresponding pad of the semiconductor ~~device~~ chip and an assigned pad of the carrier.

11. (Currently Amended) The testing method according to claim 8, wherein an amount of voltage dropping across the corresponding semiconductor ~~device~~ chip pad is determined to find whether an electric contact has been established between a corresponding pad of the semiconductor ~~device~~ chip and an assigned pad of the carrier.

12. (Currently Amended) A testing system for testing contacting between a semiconductor ~~device~~ chip and a carrier, comprising:

a testing apparatus to which a carrier can be connected, and which is configured such that contacting between the carrier and the semiconductor ~~device~~ chip is tested by the testing ~~device~~ chip immediately after loading of the carrier with a semiconductor ~~device~~ chip: and

one or more contacting test contacts exclusively to test the contacting between the semiconductor ~~device~~ chip and the carrier.

13. (Currently Amended) The testing system according to claim 12, wherein the testing apparatus performs the test after a signal is output by a loading ~~device~~ chip, the signal indicating that the carrier was loaded with the semiconductor ~~device~~ chip.

14. (Currently Amended) The testing system according to claim 12, further comprising a testing apparatus, the testing apparatus being configured such that contacting between the carrier and the semiconductor ~~device~~ chip is tested immediately after loading of the carrier with the semiconductor ~~device~~ chip.

15. (Currently Amended) The method according to claim 1, wherein the one or more contacting test contacts are not used during ordinary operation of the semiconductor ~~device~~ chip.

16. (Currently Amended) The method according to claim 15, wherein the semiconductor ~~device~~ chip further comprises at least one additional contact used during ordinary operation of the semiconductor ~~device~~ chip.

17. (Currently Amended) The method according to claim 1, wherein the one or more contacting test contacts are not used for testing the functioning of the semiconductor ~~device~~ chip.

18. (Currently Amended) The method according to claim 17, wherein the semiconductor ~~device~~ chip further comprises at least one additional contact used for testing the functioning of the semiconductor ~~device~~ chip.

19. (Currently Amended) The system according to claim 12, wherein the one or more contacting test contacts are not used during ordinary operation of the semiconductor ~~device~~ chip.

20. (Currently Amended) The system according to claim 19, wherein the semiconductor ~~device~~ chip further comprises at least one additional contact used during ordinary operation of the semiconductor ~~device~~ chip.

21. (Currently Amended) The system according to claim 12, wherein the one or more contacting test contacts are not used for testing the functioning of the semiconductor ~~device~~ chip.

22. (Currently Amended) The system according to claim 21, wherein the semiconductor ~~device~~ chip further comprises at least one additional contact used for testing the functioning of the semiconductor ~~device~~ chip.

23. (New) The testing method according to claim 1, wherein the one or more contacting test contacts are provided on a bottom of the semiconductor chip.

24. (New) The testing system according to claim 12, wherein the one or more contacting test contacts are provided on a bottom of the semiconductor chip.